REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

I. STATUS OF THE CLAIMS

Claims 10-12 are cancelled herein without prejudice or disclaimer.

Claims 1 and 6 are amended herein.

In view of the above, it is respectfully submitted that claims 1-9 are currently pending and under consideration.

II. REJECTION OF CLAIMS 1, 6, AND 10-12 UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

In item 2 on page 2 of the Office Action, claims 1, 6, and 10-12 are rejected under 35 U.S.C. § 112, second paragraph. Claims 1 and 6 are amended herein, and claims 10-12 are cancelled herein to overcome the rejection.

In view of the above, it is respectfully submitted that the rejection is overcome.

III. REJECTION OF CLAIMS 1-5 AND 7-9 UNDER 35 U.S.C. § 103(A) AS BEING UNPATENTABLE OVER ZULIAN (US 5,701,413) IN VIEW OF TSUNODA (US 6,282,688)

In item 5 on page 2 of the Office Action, claims 1-5 and 7-9 are indicated as being rejected under 35 U.S.C. § 103(a) as being unpatentable over Zulian et al. (US 5,701,413) in view of Tsunoda et al. (US 6,282,688).

According to claim 1 of the present invention, an error detection/correction system comprises "a plurality of error detection/correction code generation circuits."

Zulian et al. ("Zulian") discloses a multi-processor system, which includes a plurality of processors having access to a plurality of shared memory modules. Zulian also discloses in column 13, lines 43-47, that "[t]he outputs of the multiplexer 56 are connected to the inputs of an 8 bit code generation logic 61 for detection and correction of errors (ECC GEN) and to the inputs of a 72 bit register 62 which also receives on 8 inputs the ECC code generated by the logic 61" (see also FIG. 5 of Zulian).

However, Zulian discloses a single bit register 62 but fails to describe "a plurality of error detection/correction code generation circuits" as described in the claimed invention. In this regard, Zulian does not disclose a system having a plurality of error detection/correction code

generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity, and error detection/correction circuits corresponding to the error detection/correction code generation circuits. Therefore, it would not have been obvious to a person of ordinary skill in the art to combine Zulian and Tsunado et al. to teach the claimed plurality of error detection/correction code generation circuits as recited in claim 1 of the present invention.

Dependent claims 2-9 (depending, either directly or indirectly, from claim 1) recite patentably distinguishing features of their own, and further, are at least patentably distinguishing due to their dependencies from independent claims 1. For example, in contrast to Zulian, dependent claim 2 provides, "wherein the error detection/correction system switches over between error detection/correction codes to be used dependent upon on a phase of transmitting an address, a command, and data." The Examiner relies on column 17, lines 49 through column 18 of Zulian. However, nothing in column 17, lines 49 through column 18 of Zulian discloses the claimed features of the error detection/correction system switching over between error detection/correction codes to be used dependent upon on a phase of transmitting an address, a command, and data (see claim 2).

In view of the above, it is respectfully submitted that the rejection is overcome.

IV. CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that each of the claims patentably distinguishes over the prior art, and therefore defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowability of all pending claims are therefore respectfully requested.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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